

IN THE CLAIMS:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Amended) A circuit for use in a high speed multi-channel transmission system, which system is intended to transmit data at a rate R using K sub-channels through a channel having varying transmission characteristics, said circuit comprising:

a sub-channel parameter memory for storing data capacities associated with some or all of said sub-channels, including initial data capacities and adapted data capacities; and

a processing unit which can perform a configuration procedure to generate said initial data capacities to configure said system to operate at the data rate R ; and

said processing unit being further configured to perform a first adaptation procedure to generate said adapted data capacities within a first time period when significant changes are required in the data rate R ; and

said processing unit being otherwise configured to perform a second adaptation procedure to generate said adapted[,]data capacities within a second time period, said second time period being shorter than said first time period;

wherein the processing unit executes the configuration procedure until said data rate is achieved or until a specified iteration criteria parameter is satisfied and thereafter executes either or both of the first and second adaptation routines as needed to maintain the data rate R .

10. (Amended) The [circuit] method of claim 6, wherein said second adaptation routine is selected by said processing unit when a specified allowable system adaptation time period is relatively small.

15. (Amended) The method of claim 11, further including a step [(b)'] (b): monitoring the channel for requests for modifications to a data rate, and based on such request selecting either said first adaptation routine or said second adaptation routine.

16. (Amended) A method of controlling bit and gain loadings for sub-carriers used in a data transmission through a channel having a target data rate R and a nominal power transmission P , the method comprising the steps of:

(a) initializing the sub-channel data carriers with initial capacity parameters to achieve the target data rate R and nominal power transmission P , which initial capacity parameters are based on initial signal to noise ratios measured for the sub-channel data carriers;

(b) identifying whether any data rate changes and/or power transmission changes are requested and/or required to the target data rate R and nominal power transmission respectively,

(c) in response to any such data rate changes and/or power transmission changes identified, modifying said initial capacity parameters to generate modified capacity parameters for achieving said data rate changes and power transmission changes, such that:

a first adaptation routine is used for generating said modified capacity parameters when said data rate changes and/or said power transmission [charges] changes are significant; and

otherwise a second adaptation routine is used for generating said modified capacity parameters.

20. A data transmission method comprising:

setting a first power margin;

measuring a plurality of signal-to-noise ratios associated with a plurality of sub-channels;

determining a plurality of data capacities associated with the sub-channels at the first power margin according to the signal-to-noise ratios associated with the sub-channels, wherein the data capacities are determined through calculating a plurality of bit loadings associated with the sub-channels at the first power margin;

determining a plurality of power modification factors corresponding to the bit loadings at the first power margin;

calculating a first total bit rate according to the data capacities; and

adjusting the first total bit rate to meet a target data rate through adjusting the data capacities, wherein the data capacities are adjusted according to the bit loadings and the power modification factors.

21. The method of claim 20, further comprising verifying the bit loadings and the power modification factors at the first power margin.

22. The method of claim 20, wherein the power modification factors are determined according to at least one of the signal-to-noise ratios and a plurality of bit error rates associated with the sub-channels.

23. The method of claim 20, where the bit loadings associated with each of the sub-channels include a first bit number and a second bit number, wherein the first bit number is larger than the second bit number, and the power modification factors associated with each of the sub-channels include a first power factor corresponding to the first bit number and a second power modification factor corresponding to the second bit number.

24. The method of claim 23, wherein the data capacities are adjusted sequentially in an order determined according to the first power factor, the second power factor, the first bit number, and the second bit number associated with each of the sub-channels.

25. The method of claim 24, wherein the first bit number of bit loadings of one of the sub-channels is a data capacity of the sub-channel.

26. The method of claim 25, wherein the order is a descending order according to the difference between the first power factor and the second power factor divided by the difference between the first bit number and the second bit number associated with each of the sub-channels.

27. The method of claim 26, wherein the data capacity associated with one of the sub-channels is adjusted through substituting the first power factor with the second power factor and substituting the first bit number with the second bit number associated with the channel.

28. The method of claim 23, wherein the first bit number is a maximum bit loading and the second bit number is a minimum bit loading associated with each of the sub-channels.

29. The method of claim 28, wherein the data capacities are adjusted sequentially in an order determined according to a plurality of power adjustment values associated with the sub-channels, wherein the power adjustment values are determined by the following equation:

$$(e_{\max}(i) - e_{\min}(i)) / (b_{\max}(i) - b_{\min}(i))$$

where $b_{\min}(i)$ and $b_{\max}(i)$ respectively are the minimum and maximum bit loadings for each of the sub-channels, and $e_{\min}(i)$ and $e_{\max}(i)$ respectively are the first and second power factors respectively associated with the minimum and the maximum bit loading.

30. The method of claim 29, wherein the maximum bit loading of each sub-channel is a maximum data capacity associated with the sub-channel.

31. The method of claim 20, further comprising determining whether to enable or disable each of the sub-channels according to the bit loadings and the power modification factors.

32. The method of claim 20, the method further comprising:
determining a second power margin according to the difference between the first total bit rate and the target data rate after adjusting the first total bit rate;
calculating a second total bit rate at the second power margin according to the data capacities associated with the sub-channels at the second power margin; and
adjusting the second total bit rate through adjusting the data capacities associated with the sub-channels at the second power margin,
wherein the difference between the second total bit rate and the target data rate is smaller than the difference between the first total bit rate and the target data rate.

33. The method of claim 32, further comprising verifying the bit loadings and the power modification factors at the second power margin.

34. The method of claim 32, wherein when the target bit rate is between the first total bit rate and the second total bit rate, the method further comprises:
determining a third power margin according to the first power margin and the second power margin, wherein the third power margin is between the first power margin and the second power margin; and

calculating a third total bit rate at the third power margin according to the data capacities associated with the sub-channels at the third power margin,

wherein the difference between the third total bit rate and the target data rate is smaller than the difference between the second total bit rate and the target data rate.

35. The method of claim 32, wherein the third power margin is the square root of the product of multiplying the first power margin and the second power margin.

36. The method of claim 20, wherein the data capacities are determined and adjusted according to at least one of changes in communication system characteristics and changes in the target data rate.

37. The method of claim 36, wherein the communication system characteristics include the signal-to-noise ratios associated with the sub-channels.

38. The method of claim 20, wherein the data capacities are determined and adjusted through considering a maximum transmission power of a communication system.

39. A method of controlling data transmission comprising:
measuring a plurality of signal-to-noise ratios associated with a plurality of sub-channels;
calculating a plurality of data capacities associated with the sub-channels according to the signal-to-noise ratios; and

calculating a total bit rate according to the data capacities; and
when a target data rate is larger than the total bit rate,

calculating a plurality of first power margin factors associated with the sub-
channels, wherein each of the first power margin factors represents a power
margin factor of a sub-channel when at least one additional bit is added to the
sub-channel; and

allocating at least one bit to at least one of the sub-channels according to the
first power margin factors associated with the sub-channels.

40. The method of claim 39, further comprising repeating the steps of calculating
the first power margin factors and allocating bits until the total bit rate approximates or
equals the target data rate.

41. The method of claim 39, wherein the first power modification factors are
determined according to at least one of the signal-to-noise ratios and a plurality of bit error
rates associated with the sub-channels.

42. The method of claim 39, wherein the additional bits are allocated to the sub-
channels in an order based on the first power margin factors.

43. The method of claim 42, wherein the order is a descending order based on a
value of the first power margin factor associated with each of the sub-channels.

44. The method of claim 39, wherein when the target data rate is smaller than the total bit rate, the method further comprises:

calculating a plurality of second power margin factors associated with the sub-channels, wherein each of the second power margin factors represents a power margin factor of a sub-channel when at least one bit is removed from the sub-channel; and

dropping at least one unused bit from at least one of the sub-channels according to the second power margin factors associated with the sub-channels.

45. The method of claim 44, further comprising repeating the steps of calculating the second power margin factors and dropping bits until the total bit rate approximates or equals the target data rate.

46. The method of claim 44, wherein the second power margin factors are determined according to at least one of the signal-to-noise ratios and a plurality of bit error rates associated with the sub-channels.

47. The method of claim 44, wherein the at least one unused bit is dropped from at least one of the sub-channels in an order based on the second power margin factors.

48. The method of claim 47, wherein the order is an ascending order based on the value of the second power margin factor associated with each of the sub-channels.

49. A method for transmitting data through sub-channels, comprising:

providing a power margin;

obtaining signal-to-noise ratios associated with the sub-channels;

determining bit loading capacities and power modification factors associated with the sub-channels at the power margin according to the signal-to-noise ratios associated with the sub-channels; and

determining a total bit rate at the power margin according to at least one of the bit loading capacities and power modification factors.

50. The method of claim 49, further comprising verifying the bit loadings and the power modification factors at the power margin.

51. The method of claim 49, further comprising:

providing a target bit rate;

determining an estimated power margin according to at least one of the total bit rate and the target bit rate;

replacing the power margin with the estimated power margin; and

repeating, as a first loop, the steps of determining the bit loading capacities and the power modification factors, of determining the total bit rate, of determining the estimated power margin, and of replacing the power margin, for a predetermined number of times, until the total bit rate approximates or equals the target bit rate, or until obtaining two total bit rates that bound the target bit rate between the two total bit rates.

52. The method of claim 51, when obtaining two total bit rates that bound the target bit rate between the two total bit rates, the method further comprises:

determining an updated power margin according to the two estimated power margins associated with the two total bit rates;

replacing the power margin with the updated power margin;

repeating the first loop until obtaining the two total bit rates that bound the target bit rate and the steps of determining the updated power margin according to the two estimated power margins associated with the two total bit rates and of replacing the power margin with the updated power margin, for a predetermined number of times or until a most recent total bit rate approximates or equals the target bit rate.

53. The method of claim 52, wherein the updated power margin is the square root of the product of multiplying the two estimated power margins associated with the two total bit rates.

54. The method of claim 49, wherein determining the bit loading capacities and the power modification factors comprises determining the bit loading capacities and the power modification factors according to at least one of the signal-to-noise ratios, data rates associated with the sub-channels, a number of sub-channels having a non-zero bit capacity, and a system transmission power.

55. The method of claim 49, wherein the bit loading capacity of each sub-channel is represented by a minimum bit loading and a maximum bit loading.

56. The method of claim 49, wherein each sub-channel has a minimum power modification factor and a maximum power modification factor respectively associated with a minimum bit loading and a maximum bit loading.

57. The method of claim 49, wherein obtaining the signal-to-noise ratios includes using previously existing signal-to-noise ratios as the signal-to-noise ratios or measuring updated signal-to-noise ratios as the signal-to-noise ratios.

58. The method of claim 49, further comprising determining whether to enable or disable at least one of the sub-channels according to the bit loading capacities and the power modification factors.

59. A data transmission system comprising:
a memory to store a plurality of signal-to-noise ratios associated with a plurality of sub-channels; and
a processor configured to
determine a plurality of data capacities associated with the sub-channels at a first power margin according to the signal-to-noise ratios associated with the sub-channels,
wherein the data capacities are determined through calculating a plurality of bit loadings associated with the sub-channels at the first power margin;
determine a plurality of power modification factors corresponding to the bit loadings at the first power margin;

calculate a first total bit rate according to the data capacities; and
adjust the first total bit rate to meet a target data rate through adjusting the data
capacities, wherein the data capacities are adjusted according to the bit loadings and the
power modification factors.

60. The system of claim 59, wherein the processor is configured to verify the bit
loading and the power modification factors at the first power margin.

61. The system of claim 59, wherein the power modification factors are determined
according to at least one of the signal-to-noise ratios and a plurality of bit error rates
associated with the sub-channels.

62. The system of claim 59, wherein the bit loadings associated with each of the
sub-channels include a first bit number and a second bit number, wherein the first bit
number is larger than the second bit number, and the power modification factors
associated with each of the sub-channels include a first power factor corresponding to the
first bit number and a second power modification factor corresponding to the second bit
number.

63. The system of claim 62, wherein the data capacities are adjusted sequentially
in an order determined according to the first power factor, the second power factor, the first
bit number, and the second bit number associated with each of the sub-channels.

64. The system of claim 63, wherein the first bit number of bit loadings of one of the sub-channels is a data capacity of the sub-channel.

65. The system of claim 64, wherein the order is a descending order according to the difference between the first power factor and the second power factor divided by the difference between the first bit number and the second bit number associated with each of the sub-channels.

66. The system of claim 65, wherein the data capacity associated with one of the sub-channels is adjusted through substituting the first power factor with the second power factor and substituting the first bit number with the second bit number associated with the sub-channel.

67. The system of claim 62, wherein the first bit number is a maximum bit loading and the second bit number is a minimum bit loading associated with each of the sub-channels.

68. The system of claim 67, wherein the data capacities are adjusted sequentially in an order determined according to a plurality of power adjustment values associated with the sub-channels, wherein the power adjustment values are determined by the following equation:

$$(e_{\max(i)} - e_{\min(i)}) / (b_{\max(i)} - b_{\min(i)})$$

where $b_{min}(i)$ and $b_{max}(i)$ respectively are the minimum and maximum bit loadings for each of the sub-channels, and $e_{min}(i)$ and $e_{max}(i)$ respectively are the first and second power factors respectively associated with the minimum and the maximum bit loadings.

69. The system of claim 68, wherein the maximum bit loading of each sub-channel is the maximum data capacity associated with the sub-channel.

70. The system of claim 59, wherein the processor is configured to determine whether to enable or disable each of the sub-channels according to the bit loadings and the power modification factors.

71. The system of claim 59, wherein the processor is configured to determine a second power margin according to the difference between the first total bit rate and the target data rate;

calculate a second total bit rate at the second power margin according to the data capacities associated with the sub-channels at the second power margin; and

adjust the second total bit rate through adjusting the data capacities,

wherein the difference between the second total bit rate and the target data rate is smaller than the difference between the first total bit rate and the target data rate.

72. The system of claim 71, wherein the processor is configured to verify the bit loading and the power modification factors at the second power margin.

73. The system of claim 71, wherein when the target bit rate is between the first total bit rate and the second total bit rate, the processor is configured to determine a third power margin according to the first power margin and the second power margin, wherein the third power margin is between the first power margin and the second power margin; and calculate a third total bit rate at the third power margin according to the data capacities associated with the sub-channels at the third power margin, wherein the difference between the third total bit rate and the target data rate is smaller than the difference between the second total bit rate and the target data rate.

74. The system of claim 73, wherein the third power margin is the square root of the product of multiplying the first power margin and the second power margin.

75. The system of claim 59, wherein the data capacities are determined and adjusted according to at least one of changes in communication system characteristics and changes in the target data rate.

76. The system of claim 75, wherein the communication system characteristics include the signal-to-noise ratios associated with the sub-channels.

77. The system of claim 59, wherein the data capacities are determined and adjusted through considering a maximum transmission power of a communication system.

78. A system of controlling data transmission comprising:
a memory to store a plurality of signal-to-noise ratios associated with a plurality of
sub-channels; and
a processor configured to
calculate a plurality of data capacities associated with the sub-channels according
to the signal-to-noise ratios; and
calculate a total bit rate according to the data capacities; and
when a target data rate is larger than the total bit rate, the processor is configured to
calculate a plurality of first power margin factors associated with the sub-
channels, wherein each of the first power margin factors represents a power
margin factor of a sub-channel when at least one bit is added to the sub-
channel; and
allocate at least one additional bit to at least one of the sub-channels
according to the first power margin factors associated with the sub-channels.

79. The system of claim 78, the processor is configured to repeat calculating the
plurality of first power margin factors and allocate at least one additional bit until the total
bit rate approximates or equals the target data rate.

80. The system of claim 78, wherein the first power modification factors are
determined according to at least one of the signal-to-noise ratios and a plurality of bit error
rates associated with the sub-channels.

81. The system of claim 78, wherein the additional bits are allocated to the sub-channels in an order based on the first power margin factors.

82. The system of claim 81, wherein the order is a descending order based on the value of the first power margin factor associated with each of the sub-channels.

83. The system of claim 78, wherein when the target data rate is smaller than the total bit rate, the processor is configured to

calculate a plurality of second power margin factors associated with the sub-channels, wherein each of the second power margin factors represents a power margin factor of a sub-channel when at least one bit is removed from the sub-channel; and

drop at least one unused bit from at least one of the sub-channels according to the second power margin factors associated with the sub-channels.

84. The system of claim 83, wherein the second power modification factors are determined according to at least one of the signal-to-noise ratios and a plurality of bit error rates associated with the sub-channels.

85. The system of claim 83, wherein the processor is configured to repeat calculating the second power margin factors and dropping the at least one unused bit until the total bit rate approximates or equals the target data rate.

86. The system of claim 85, wherein the at least one unused bit is dropped from at least one of the sub-channels in an order based on the second power margin factors.

87. The system of claim 86, wherein the order is an ascending order based on the value of the second power margin factor associated with each of the sub-channels.

88. A system for transmitting data through sub-channels, comprising:
a memory to store signal-to-noise ratios associated with the sub-channels; and
a processor configured to
determine bit loading capacities and power modification factors associated with the
sub-channels at the power margin according to the signal-to-noise ratios associated with a
plurality of sub-channels; and
determine a total bit rate at the power margin according to the bit loading capacities.

89. The system of claim 88, wherein the processor is configured to verify the bit loadings and the power modification factors at the power margin.

90. The system of claim 88, wherein the processor is configured to
determine an estimated power margin according to at least one of the total bit rate
and a target bit rate;
replace the power margin with the estimated power margin; and
repeat a first loop of determining the bit loading capacities and the power
modification factors, determining the total bit rate, determining the estimated power

margin, and replacing the power margin, for a predetermined number of times, until the total bit rate approximates or equals the target bit rate, or until obtaining two total bit rates that bound the target bit rate between the two total bit rates.

91. The system of claim 90, when obtaining two total bit rates that bound the target bit rate between the two total bit rates, the processor is configured to
determine an updated power margin according to the two estimated power margins associated with the two total bit rates;
replace the power margin with the updated power margin;
repeat the first loop until obtaining the two total bit rates that bound the target bit rate, determine the updated power margin according to the two estimated power margins associated with the two total bit rates, and replace the power margin with the updated power margin, for a predetermined number of times or until a most recent total bit rate equals the target bit rate.

92. The system of claim 91, wherein the updated power margin is the square root of the product of multiplying the two estimated power margins associated with the two total bit rates.

93. The system of claim 88, wherein the processor is configured to determine the bit loading capacities and the power modification factors according to at least one of the signal-to-noise ratios, data rates associated with the sub-channels, number of sub-channels having a non-zero bit capacity, and a system transmission power.

94. The system of claim 88, wherein the bit loading capacity of each sub-channel is represented by a minimum bit loading and a maximum bit loading.

95. The system of claim 88, wherein each sub-channel has a minimum power modification factor and a maximum power modification factor respectively associated with a minimum bit loading and a maximum bit loading.

96. The system of claim 88, wherein the processor is configured to determine whether to enable or disable at least one of the sub-channels according to the bit loadings and the power modification factors.

97. A device to transmit data through sub-channels, comprising:
circuitry to determine bit loading capacities and power modification factors
associated with the sub-channels at the power margin; and
circuitry to determine a total bit rate at the power margin according to the bit loading capacities.

98. The device of claim 97, further comprising:
circuitry to determine an estimated power margin according to at least one of the
total bit rate and a target bit rate;
circuitry to replace the power margin with the estimated power margin; and

circuitry to repeat a first loop of determining the bit loading capacities and the power modification factors, determining the total bit rate, determining the estimated power margin, and replacing the power margin, for a predetermined number of times, until the total bit rate approximates or equals the target bit rate, or until obtaining two total bit rates that bound the target bit rate between the two total bit rates.

99. A method for configuring a device to transmit data through sub-channels, comprising:

configuring the device to determine bit loading capacities and power modification factors associated with the sub-channels at a power margin; and

configuring the device to determine a total bit rate at the power margin according to the bit loading capacities.

100. The method of claim 99, further comprising:

configuring the device to determine an estimated power margin according to at least one of the total bit rate and the target bit rate;

configuring the device to replace the power margin with the estimated power margin; and

configuring the device to repeat the first loop of determining the bit loading capacities and the power modification factors, determining the total bit rate, determining the estimated power margin, and replacing the power margin, for a predetermined number of times, until the total bit rate approximates or equals the target bit rate, or until obtaining two total bit rates that bound the target bit rate between the two total bit rates.